

Application No. 10/699,766

MXIC 1522-1  
(P900383)In the claims:

This listing of claims will replace all prior versions and listings of claims in the application:

## 1. (original) An integrated circuit, comprising:

a configurable logic array having a programmable configuration defined by configuration data stored in electrically programmable configuration points within the configurable logic array;

a programmable configuration memory, adapted to store the configuration data; memory adapted to store instructions for a mission function for the integrated circuit, and to store instructions for a configuration function used to transfer the configuration data from the configuration memory to the programmable configuration points within the configurable logic array; and

a processor coupled to the memory which fetches and executes instructions from the memory.

2. (original) The integrated circuit of claim 1, wherein said memory comprises a non-volatile store.

3. (original) The integrated circuit of claim 1, wherein said memory comprises a floating gate memory store.

4. (original) The integrated circuit of claim 1, wherein said memory comprises a read-only memory store.

5. (original) The integrated circuit of claim 1, wherein said memory comprises a first non-volatile store for the configuration function, and a second store for the mission function.

6. (original) The integrated circuit of claim 1, wherein said memory comprises a first volatile store for the configuration function, and a second store for the mission function.

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7. (original) The integrated circuit of claim 1, including a watchdog timer coupled to the processor, and wherein the configuration function includes using the watchdog timer.
8. (original) The integrated circuit of claim 1, wherein the configuration function includes loading the programmable configuration memory via an input port on the integrated circuit.
9. (original) The integrated circuit of claim 1, wherein the configuration function includes receiving encrypted configuration data via an input port on the integrated circuit, decrypting the configuration data, and loading the programmable configuration memory with decrypted configuration data.
10. (original) The integrated circuit of claim 1, wherein the configuration function includes receiving compressed configuration data via an input port on the integrated circuit, decompressing the configuration data, and loading the programmable configuration memory with decompressed configuration data.
11. (original) The integrated circuit of claim 1, wherein the programmable configuration memory comprises a non-volatile store.
12. (original) The integrated circuit of claim 1, wherein the programmable configuration memory comprises a volatile store.
13. (original) The integrated circuit of claim 1, wherein the electrically programmable configuration points comprise non-volatile, charge programmable memory cells.
14. (original) The integrated circuit of claim 1, wherein the configuration function includes loading the programmable configuration memory via an input port on the integrated circuit, and including:

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an interface between the processor and the configuration memory supporting said loading; and

an interface between the configuration memory and the configurable logic array supporting said transfer of configuration data to the configurable logic array.

~~16.~~ 15. The integrated circuit of claim 1, wherein the configuration function includes loading the programmable configuration memory via an input port on the integrated circuit, and including:

an interface between the processor and the configuration memory supporting said loading and said transfer of configuration data to the configurable logic array; and

an interface between the processor and the configurable logic array supporting said transfer of configuration data to the configurable logic array.

17. (canceled).

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